Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of forming an interconnect between a first layer copper line and a second layer copper line of a semiconductor circuit, said method comprising:

forming a via through a first dielectric layer to expose the surface of the first layer copper line;

depositing a first barrier layer over inner sidewall and bottom surfaces of the via, the barrier layer providing a diffusion barrier against copper;

etching selectively the bottom surface of the via to substantially eliminate the barrier layer from the bottom surface, wherein said etching selectively is performed in a physical vapor deposition (PVD) tool; and

after etching selectively the bottom surface of the via, depositing a second barrier layer over the inner surfaces of the via including the bottom surface of the via, the second barrier layer providing a diffusion barrier against copper and ensures sufficient wettability of copper.

2. (original) The method of claim 1 further comprising forming a trench in the dielectric layer, a portion of which lies substantially over the via; wherein the first and second barrier layers are deposited on inner surfaces of the trench.

3. (original) The method of claim 1 further comprising the step of depositing copper in the inner surfaces of the via and trench, thereby substantially filling the via and trench with the deposited copper.

4. (original) The method of claim 1 wherein the first barrier layer is a conformal barrier layer.

5. (previously presented) A method of forming an interconnect between a first layer copper line and a second layer copper line of a semiconductor circuit, said method comprising:

forming a via through a first dielectric layer to expose the surface of the first layer copper line;

depositing a first barrier layer over inner sidewall and bottom surfaces of the via, the barrier layer providing a diffusion barrier against copper;

etching selectively the bottom surface of the via to substantially eliminate the barrier layer from the bottom surface; and

depositing a second barrier layer over the inner surfaces of the via, the second barrier layer providing a diffusion barrier against copper and ensures sufficient wettability of copper, wherein the first barrier layer is a conformal barrier layer and wherein the conformal barrier layer is a layer of plasma+silane treated CVD TiNSi.

6. (original) The method of claim 4 wherein the conformal barrier layer is an ALD layer of TaN.

7. (original) The method of claim 1 wherein the first barrier layer is an ionized PVD layer of at least one of the following materials: Ta, TaN.

8. (original) The method of claim 1 wherein the first barrier layer comprises at least one of the following materials: TiNSi, Ta, TaN, TaSiN, Ti, TiN, W, WN, WSiN, WCN, and Ru.

9. (original) The method of claim 1 wherein the selective etching is performed in a PVD barrier chamber.

10. (original) The method of claim 1 wherein the second barrier layer is a flash PVD layer of Ta.

11. (original) The method of claim 1 wherein the flash barrier layer is a PVD layer of Ta and wherein depositing the second barrier layer is performed in the same PVD barrier chamber as the selective etching.

12. (original) The method of claim 1 wherein the second barrier layer has lower resistivity with respect to the first barrier layer.

Claims 13-21. (cancelled)